WHAT IS CLAIMED IS:

1. A storage method of a memory device comprising memory cells (M1 through M16) adapted to have 2^1 states for the first write operation, 2^2 states for the second write operation and $2^k = n$ states (k, n representing respective natural numbers) for the n-th write operation, said method comprising:

storing data of the first logic level or of the second logic level in data storage circuits in the k-th write operation;

modifying the state "i-1" (I ≦ n-1, i being a natural number) of said memory cells to state "i" when the data of said data storage circuits are of the first logic level but maintaining the state of said memory cells when the data of said data storage circuits are of the second logic level;

shifting the state of said data storage circuits from the first logic level to the second logic level when the state of said memory cells has already got to state "i" and currently is at any of "0" through "i";

holding the state of said data storage circuits to the first logic level when the state of said memory cells has not got to state "i" yet and currently is at any of "0" through "i";

holding the data of said data storage circuits when the state of said memory cells is at any of "i+1" through "n-1"; and

controlling the state of said memory cells so as not to be modified from "i+1" to "n-1" even temporarily when the state of said memory cells is modified from "i-1" to "i".

2. A method according to claim 1, wherein

said control step comprising setting the state of said memory cells are set to state "0" of state "n/2" according to the externally input first data, setting the state of said memory cells to state "n/4" or "3n/4" according to the externally input second data, setting the state of said memory cells to state "n/8", "3n/8", "5n/8" or "7n/8" according to the externally input third data and, in a similar manner, setting the state of said memory cells to state "$n/2^k$", "$3n/2^k$", "$5n/2^k$", ..., "$(2^{k-1})n/2^k$".

3. A method according to claim 1, wherein

a verify operation for verifying a state by far smaller than state "i" is omitted when conducting an operation of verifying if said state "i" ($i \leqq n-1$, i being a natural number) is attained or not.

4. A method according to claim 1, wherein

a verify operation for verifying a state by far greater than state "i" is omitted when conducting an operation of verifying if said state "i" ($i \leqq n-1$, i being a natural number) is attained or not.

5. A method according to claim 1, wherein

said memory cells comprise non-volatile

semiconductor memory cells.

6. A method according to claim 1, wherein said n states are discriminated by different threshold voltages of said non-volatile semiconductor memory cells.

7. A semiconductor memory device comprising:

memory cells having n states including state "0", state "1", ... and state "n-1" (2 ≦ n, n being a natural number);

a first data storage circuit for storing externally input data, said data being of the first logic level or of the second logic level;

read circuits for reading the state of said memory cells;

a second data storage circuit for storing data of the first logic level when the state of said memory cells read out by said read circuits is at any of "0" through "i" but storing data of the second logic level when the state of said memory cells read out by said read circuits is at any of "i" through "n-1";

write circuits for modifying the state of the memory cells from state "i-1" to state "1" when the data of said first data storage circuit are of the first logic level but holding the state of the memory cells when the data of said first data storage circuit are of the second logic level;

a write verify circuit for shifting the data of

said first data storage circuit from the first logic level to the second logic level when the state of said memory cells has already got to state "i" and the data of said second data storage circuit are of the first logic level but holding the data of said first data storage circuit when the state of said memory cells has not got to state "i" yet and the data of said second data storage circuit are of the first logic level and also when the data of said second data storage circuit are of the second level; and

a write state control circuit for controlling the sate of said memory cells so as not to be modified from "i+1" to "n-1" even temporarily when the state of said memory cells is modified from "i-1" to "i".

8. A device according to claim 7, further comprising:

a first transfer means connected to said first data storage circuit for taking in external data; and

a second transfer means connected to said first data storage circuit for externally transferring the data read out from said memory cells.

9. A device according to claim 7, wherein

said memory cells comprise non-volatile semiconductor memory cells.

10. A device according to claim 7, wherein

said externally input data include the first data, the second data and the third data;

said first data being data for setting the state of said memory cells are set to state "0" of state "n/2";

said second data being data for setting the state of said memory cells to state "n/4" or "3n/4";

said third data being data for setting the state of said memory cells to state "n/8", "3n/8", "5n/8" or "7n/8".

11. A semiconductor memory device comprising:

memory cells having n states including state "0", state "1", ... and state "n-1" ($2 \leq n$, n being a natural number);

a differential amplifier circuit having at least a differential amplifier for being fed with the potential output from said memory cells at the first input terminal thereof and a reference potential different from said potential at the second input terminal thereof;

a logic circuit for selectively taking out the output signal of said at least one differential amplifier;

a data storage circuit connected to said memory cells for storing data of the first logic level or of the second logic level; and

control circuits for modifying the state of said memory cells from "i-1" to "i" when the data of said data storage circuit are of the first logic level,

maintaining the state of said memory cells when the data of said data storage circuit are of the second logic level, shifting the data of said data storage circuit from the first logic level to the second logic level when the state of said memory cells have already got to state "i" and currently is at any of "1" through "i", holding the data of said data storage circuit to the first logic level when the state of said memory cells have not got to state "i" yet and currently is at any of "1" through "i", holding the data of said data storage circuit when the state of said memory cells are at any of "i+1" through "n-1" and controlling the sate of said memory cells so as not to be modified from "i+1" to "n-1" even temporarily when the state of said memory cells is modified from "i-1" to "i".

12. A device according to claim 11, further comprising:

a first transfer means connected to said data storage circuit for transferring the data stored in said data storage circuit to said differential amplifier section and said logic circuit; and

a second transfer means connected to said data storage circuit for transferring the data detected by said differential amplifier section and said logic circuit to said data storage circuit.

13. A device according to claim 12, further comprising:

a selector for selectively connecting said data storage circuit to differential amplifier sections and logic circuits, the number of said differential amplifier sections and said logic circuits being smaller than the number of data storage circuits.

14. A device according to claim 12, wherein said memory cells comprise non-volatile semiconductor memory cells having negative threshold voltages.

15. A device according to claim 14, wherein the voltages read out from said memory cells correspond to the threshold voltages of said memory cells.

16. A device according to claim 11, wherein said externally input data include the first data, the second data and the third data;

said first data being data for setting the state of said memory cells are set to state "0" of state "n/2";

said second data being data for setting the state of said memory cells to state "n/4" or "3n/4";

said third data being data for setting the state of said memory cells to state "n/8", "3n/8", "5n/8" or "7n/8".

17. A storage method of a memory device comprising memory cells adapted to have n-valued states, said method comprising:

storing externally input data of the first logic level or of the second logic level in the data storage circuits of the device;

shifting the logic level stored in said data storage circuits in response to the first logic level or the second logic level read out from said memory cells; and

modifying the state of said memory cells when said shifted logic level stored in said data storage circuits is the first logic level but holding the state of said memory cells when said shifted logic level stored in said data storage circuits is the second logic level.

18. A method according to claim 17, wherein

said externally input data include the first data, the second data and the third data;

said first data being data for setting the state of said memory cells are set to state "0" of state "n/2";

said second data being data for setting the state of said memory cells to state "n/4" or "3n/4";

said third data being data for setting the state of said memory cells to state "n/8", "3n/8", "5n/8" or "7n/8".

19. A storage method of a memory device comprising memory cells adapted to have k-bit n-valued states ($=2^k$), said method comprising:

storing externally input data of the first logic level or of the second logic level in said data storage circuits; and

determining the state of said memory cells so as to discriminate a 1-bit state from an n-valued state by means of the smallest integer greater than $(2^k-1)/k$ according to the data stored in said data storage circuits.

20. A method according to claim 19, wherein

said externally input data include the first data, the second data and the third data;

said first data being data for setting the state of said memory cells are set to state "0" of state "n/2";

said second data being data for setting the state of said memory cells to state "n/4" or "3n/4";

said third data being data for setting the state of said memory cells to state "n/8", "3n/8", "5n/8" or "7n/8".